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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/731,850	12/09/2003	Homero L. Guimaraes	1280-SC12863ZC	4424
34814 7590 02/06/2008 LARSON NEWMAN ABEL POLANSKY & WHITE, LLP 5914 WEST COURTYARD DRIVE SUITE 200 AUSTIN, TX 78730			EXAMINER FLORES, LEON	
			ART UNIT 2611	PAPER NUMBER
			MAIL DATE 02/06/2008	DELIVERY MODE PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

# Office Action Summary

Application No.

10/731,850

Applicant(s)

TH  
GUIMARAES, HOMERO L.

Examiner

Leon Flores

Art Unit

2611

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 22 January 2008.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-3, 7-10 and 14-16 is/are rejected.
- 7) ☒ Claim(s) 4-6, 11-13, 17-20 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: \_\_\_\_\_

## **DETAILED ACTION**

### ***Response to Arguments***

1. Applicant's arguments with respect to claims (1, 9, 16) have been considered but are moot in view of the new ground(s) of rejection.

### ***Response to Remarks***

Applicant asserts that, "the claims are rejected because the Office "does not see the advantage" of each of these elements missing from the disclosures of the cited references. Office Action, p. 2, 3, 5. Applicant respectfully submits that there is no requirement under 35 U.S.C. § 103 that a claim have a particular advantage over cited art. The Office cites no other support for its requirement that the Applicant demonstrate the advantage of a particular claim element missing from the prior art. Applicant respectfully submits that the Office's implied requirement of an "advantage" under Section 103 is improper, and requests withdrawal of the Section 103 rejections premised on this requirement".

The examiner respectfully disagrees. The examiner strongly believe that applicant's claimed invention is not new since the only difference between applicant's invention, as claimed, and Nonoyama, is that applicant's offset voltage is charged at the same time (phase 2) while is being transferred to the inputs of the integrator. On the other hand, Nonoyama's offset voltage is charged and transferred in two different phases. Both methods accomplish their main objective - correct/compensate for DC offsets. However, taking the contrary, the examiner has issued a new ground of rejection in order to substantiate for this minor deficiency.

**Claim Rejections - 35 USC § 103**

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

**1. Claims (1-3, 7, 14 & 16) are rejected under 35 U.S.C. 103(a) as being unpatentable over Baird (US Patent 6,204,787 B1) in view of Nonoyama et al. (hereinafter Nonoyama) (US Patent 6,529,015), and further in view of Rabbi. (US Patent 6,313,685 B1)**

Re claim 1, Baird discloses a sigma delta converter comprising: an integrator circuitry including an integrator input and an integrator output, wherein an input signal coupled to the integrator input has an input AC voltage component and a DC offset component (In Baird, see fig. 7A: 706 & 707, col. 7, lines 48-50); a pair of capacitors

coupled to the integrator input (In Baird, see fig. 7A: 707a & 707b); a first set of switches coupled to the pair of capacitors, the first set of switches configured to transfer a first charge to the pair of capacitors during a first phase, the first charge proportional to a reference voltage (In Baird, see fig. 7B & col. 7, lines 59-61); and a second set of switches coupled between the pair of capacitors and the integrator input. (In Baird, see fig. 7B: 712a 712b)

But the reference of Baird fails to specifically teach that the second set of switches configured to transfer the first charge and a second charge to the integrator input during a second phase, the second charge proportional to the DC offset component.

However, Nonoyama does. (See fig. 1: elements 3, 4, 5 & col. 6, line 18 – col. 7, line 6) In the same field of endeavor, Nonoyama discloses a second set of switches (switches a) configured to transfer the first charge and a second charge to the integrator input during a second phase, the second charge proportional to the DC offset component.

Taking the combined teachings of Baird and Nonoyama as a whole, it would have been obvious to one of ordinary skills in the art to have incorporated theses features into the system of Baird, in the manner as claimed and as taught by Nonoyama, for the benefit of providing offset compensation.

The combination of Baird and Nonoyama discloses the limitations as claimed above, except they fail to explicitly teach that the second charge proportional to the DC offset component and based on a voltage applied in series with the pair of capacitors

during the second phase.

However, Rabbi does. (See figs 3 & 4 & col. 4, lines 42-50 & col. 5, lines 51-67 & col. 6, lines 45-56) Rabbi discloses that the second charge (348 & 350) proportional to the DC offset component and based on a voltage applied in series with the pair of capacitors during the second phase. (430 & 440 "phase 2" & col. 3, lines 1-3 & col. 4, lines 42-50)

Taking the combined teachings of Baird, Nonoyama, and Rabbi as a whole, it would have been obvious to one of ordinary skills in the art to have incorporated theses features into the system of Baird, in the manner as claimed and as taught by Nonoyama, for the benefit of providing offset compensation.

Re claim 2, the combination of Baird, Nonoyama, and Rabbi further discloses the sigma delta converter, as recited in claim 1, further comprising: a comparator coupled to the integrator circuitry output, the comparator including a comparator output. (In Baird, see fig. 4B)

Re claim 3, the combination of Baird, Nonoyama, and Rabbi further discloses the sigma delta converter, as recited in claim 1, wherein the integrator circuitry comprises N integrators coupled in series forming an Nth-Order sigma delta loop filter, each of the N integrators having a first input, a second input, a first output and a second output, each of the N integrators having a first integrator capacitor coupled to the first input and the first output and a second integrator capacitor coupled to the second input and the

second output. (In Baird, see fig. 4B & col. 6, lines 33-37)

Re claim 7, the combination of Baird, Nonoyama, and Rabbi further discloses the sigma delta converter, as recited in claim 1, wherein the integrator is a continuous time integrator. (In Baird, see fig. 4B & col. 6, lines 34-37. Furthermore, since the signal is being integrated three times the signal is converted to digital until the last stage of the 3rd order modulator by an ADC.)

Claim 14 has been analyzed and rejected w/r to claim 7 above.

Claim 16 is a method claim corresponding to system claim 1. Hence, the steps performed in method claim 16 would have necessitated the elements in system claim 1. Therefore, claim 16 has been analyzed and rejected w/r to claim 1 above.

**2. Claims (8 & 15) are rejected under 35 U.S.C. 103(a) as being unpatentable over Baird (US Patent 6,204,787 B1), Nonoyama et al. (hereinafter Nonoyama) (US Patent 6,529,015), and Rabbi. (US Patent 6,313,685 B1), as applied to claim 1 above, and further in view of Ferguson, Jr. et al (hereinafter Ferguson) (US Patent 6,040,793)**

Re claim 8, the combination of Baird, Nonoyama, and Rabbi fails to explicitly teach that wherein the integrator is a discrete time integrator.

However, Ferguson does. (See col. 1, lines 50-56) Ferguson discloses the

integrator is a discrete time integrator. Furthermore, the output of the integrator clocked, latched comparator.

Taking the combined teachings of Baird, Nonoyama, Rabbi, and Ferguson as a whole, it would have been obvious to one of ordinary skills in the art to have incorporated these features into the system of Baird, as modified by Nonoyama and Rabbi, in the manner as claimed and as taught by Ferguson, for the benefit of providing compensation.

Claim 15 has been analyzed and rejected w/r to claim 8 above.

**Claims (9-10) are rejected under 35 U.S.C. 103(a) as being unpatentable over Baird (US Patent 6,204,787 B1), Nonoyama et al. (hereinafter Nonoyama) (US Patent 6,529,015), and Rabbi. (US Patent 6,313,685 B1), as applied to claim 1 above, and further in view of Bazarjani et al. (hereinafter Bazarjani) (US Patent 6,005,506)**

1. Re claim 9, Baird discloses a radio frequency (RF) signal receive path comprising: an integrator circuitry including an integrator input and an integrator output, wherein an input signal coupled to the integrator input has an input AC voltage component and a DC offset component (In Baird, see fig. 7A: 706 & 707, col. 7, lines 48-50); a pair of capacitors coupled to the integrator input (In Baird, see fig. 7A: 707a & 707b); a first set of switches coupled the pair of capacitors, the first set of switches configured to transfer a first charge to the pair of capacitors during a first phase, the first



charge proportional to a reference voltage (In Baird, see fig. 7B & col. 7, lines 59-61); and a second set of switches coupled to the pair of capacitors. (In Baird, see fig. 7B: 712a 712b)

But the reference of Baird fails to specifically teach that the second set of switches configured to transfer the first charge and a second charge to the integrator input during a second phase, the second charge proportional to the DC offset component and based on a voltage applied in series with the pair of capacitors during the second phase.

However, Nonoyama does. (See fig. 1: elements 3, 4, 5 & col. 6, line 18 – col. 7, line 6) In the same field of endeavor, Nonoyama discloses a second set of switches (switches a) configured to transfer the first charge and a second charge to the integrator input during a second phase, the second charge proportional to the DC offset component.

Taking the combined teachings of Baird and Nonoyama as a whole, it would have been obvious to one of ordinary skills in the art to have incorporated theses features into the system of Baird, in the manner as claimed and as taught by Nonoyama, for the benefit of providing offset compensation.

The combination of Baird and Nonoyama discloses the limitations as claimed above, except they fail to explicitly teach that the second charge proportional to the DC offset component and based on a voltage applied in series with the pair of capacitors during the second phase.

However, Rabbi does. (See figs 3 & 4 & col. 4, lines 42-50 & col. 5, lines 51-67

& col. 6, lines 45-56) Rabbi discloses that the second charge (348 & 350) proportional to the DC offset component and based on a voltage applied in series with the pair of capacitors during the second phase. (430 & 440 "phase 2" & col. 3, lines 1-3 & col. 4, lines 42-50)

Taking the combined teachings of Baird, Nonoyama, and Rabbi as a whole, it would have been obvious to one of ordinary skills in the art to have incorporated these features into the system of Baird, in the manner as claimed and as taught by Nonoyama, for the benefit of providing offset compensation.

The combination of Baird, Nonoyama, and Rabbi discloses the limitations as claimed above, except they fail to specifically teach an intermediate frequency amplifier (IFA) including an IFA output; a plurality of anti-aliasing filters (AAFs) coupled to the IFA output, the AAFs having an AAF output; and a sigma delta converter coupled to the AAF output.

However, Bazarjani does. (See fig. 6 & col. 13, lines 41-61) Bazarjani discloses an intermediate frequency amplifier (IFA) including an IFA output (2426), a plurality of anti-aliasing filters (AAFs) coupled to the IFA output, the AAFs having an AAF output (2430a & 2430b); and a sigma delta converter coupled to the AAF output. (2440a & 2440b)

Taking the combined teachings of Baird, Nonoyama, Rabbi, and Bazarjani as a whole, it would have been obvious to one of ordinary skills in the art to have incorporated these features into the system of Baird, as modified by Nonoyama and Rabbi, in the manner as claimed and as taught by Bazarjani, for the benefit of providing

gain control, match filtering and/or anti-alias filtering, and to produce digitized baseband samples.

Re claim 10, the combination of Baird, Nonoyama, Rabbi, and Bazarjani further discloses the RF signal receive path, as recited in claim 9, wherein the integrator circuitry comprises N integrators coupled in series forming an Nth-Order sigma delta converter, each of the N integrators having a first input, a second input, a first output and a second output, each of the N integrators having a first integrator capacitor coupled to the first input and the first output and a second integrator capacitor coupled to the second input and the second output. (In Baird, see fig. 4B & col. 6, lines 33-37)

### **Allowable Subject Matter**

3. Claims (4-6, 11-13, 17-20) are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

### **Contact**

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leon Flores whose telephone number is 571-270-1201. The examiner can normally be reached on Mon-Fri 7-5pm Alternate Fridays off.


If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Payne can be reached on 571-272-3024. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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LF  
January 31, 2008

  
DAVID C. PAYNE  
SUPERVISORY PATENT EXAMINER